Evaluation of Delay PUFs on CMOS 65 nm Technology: ASIC vs FPGA

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Abstract

This work presents a comparison between the performance of two types of silicon Physically Unclonable Functions (PUFs), namely the arbiter and the loop PUFs. The arbiter and the loop PUF are designed on two CMOS-65nm technology platforms: ASIC and FPGA (Xilinx Virtex-5). A mixed PUF design is proposed to allow a fair comparison between the two structures. The principal of the mixed PUF design consists on the use of the same delay chains on both arbiter and loop PUF structures. The comparison analysis reveals that the arbiter PUF structure has the worst performance when compared to the loop PUF, on both platforms. We also observe that the performance for both structures are better when designed on ASIC.