

# IP Watermark Verification Based on Power Consumption Analysis

Cédric Marchand, Lilian Bossuet, Edward Jung

## Abstract

The increasing production costs of electronic devices and changes in the design method of integrated circuits (ICs) has led to emerging threats in the microelectronic industry. Today, high value chips are the target of counterfeiting, theft and malicious hardware insertion (such as hardware trojans). Intellectual property (IP) protection has become a major concern and we propose to fight counterfeiting and theft by designing salutary hardware (salware). Instead of insert malicious effect inside ICs like malware (e.g. hardware trojan), a salware uses the same techniques, strategies and means to bring IP protections. One of the most studied salware is IP watermarking. Many works propose to target the finite state machine of digital IP to perform the watermarking. But, most of the time, the verification of the watermark is not clearly proposed. This conduces to a lack of credibility of these works. This paper proposes a watermark verification scheme using a correlation analysis based on the measurement of the IC power consumption. This article mainly presents this process of verification and also discusses about its parameters according to experimental results.