Secure partial dynamic reconfiguration of FPGAs

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Abstract

This talk discusses the use and security of partial dynamic reconfiguration on reconfigurable devices, in particular Xilinx FPGA. The secure partial dynamic reconfiguration on SRAM based FPGAs can significantly impact the reconfiguration process and the available resources on the device, given the complex multi-layered partial bitstream validation process. This can adversely affects the performance of applications using reconfigurable hardware.
This talk will start with an overview on the native Xilinx reconfiguration process and the inbuilt security mechanisms. Following the existing approaches, methods, and trade-offs considered by each one will be discussed.