Reversible Denial-of-Service by Locking Gates Insertion for IP Cores Design Protection

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Abstract

Nowadays, electronics systems design is a complex process. A design-and-reuse model has been adopted, and the vast majority of designers integrates third party intellectual property (IP) cores in their design in order to reduce time to market. Due to their immaterial form and high market value, IP cores are exposed to threats such as cloning and illegal copying. In order to fight these threats, we propose to achieve functional locking, equivalent to a triggerable and reversible denial-of-service. This is done by inserting locking gates at specific locations in the netlist, allowing to force outputs at a fixed value. We developed a new method based on graph exploration techniques for locking gates insertion. It selects candidate nodes ten thousand times faster than state-of-the-art fault analysis-based logic masking techniques. Methods are then compared on ISCAS'85 combinational benchmarks.