

Asynchronous S-Boxes

Designing Clockless First-Order Masked Functions

Mateus Simoes^{1,2}, Lilian Bossuet¹, Nicolas Bruneau², Vincent Grosso¹,
Patrick Haddad² and Thomas Sarno²

¹ Laboratoire Hubert Curien, Saint-Etienne, France

{[mateus.simoes](mailto:mateus.simoes@univ-st-etienne.fr), [lilian.bossuet](mailto:lilian.bossuet@univ-st-etienne.fr), [vincent.grosso](mailto:vincent.grosso@univ-st-etienne.fr)}@univ-st-etienne.fr

² STMicroelectronics, Rousset, France {[nicolas.bruneau](mailto:nicolas.bruneau@st.com), [patrick.haddad](mailto:patrick.haddad@st.com)}@st.com

Abstract. Passive physical attacks represent a threat to microelectronics systems by exploiting leakages through side-channels, such as power consumption and electromagnetic radiation. In this context, masking is a sound countermeasure against side-channel attacks, which splits the secret data into several randomly uniform data, achieving independence between the data processing and the secret variable. However, a secure masking scheme requires additional implementation costs. Furthermore, glitches and early evaluation can temporally weaken a masked implementation in hardware, creating a potential source of exploitable leakages.

This work shows how to create register-free masking schemes that avoid the early evaluation effect with the help of the dual-rail logic. Moreover, we employ monotonic functions with the purpose of eliminating the occurrence of glitches in combinational circuits. Finally, we evaluate different 2-share masked implementations of the PRESENT and AES S-boxes in a noiseless scenario in order to detect potential first-order leakages and to determine data propagation profiles correlated to the secret variables.